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| 09/941,861 | 08/30/2001 | Tsutomu Iwaki | 04329.2626 | 7542 |

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| EXAMINER | |
|---|---|
| STOYNOV, STEFAN | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2116 | |

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Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/941,861 | IWAKI, TSUTOMU | |
| | Examiner | Art Unit | |
| | Stefan Stoynov | 2116 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *30 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-5,7-9,12,13,15-17 and 19-21* is/are rejected.

7)☒ Claim(s) *2,6,10,11,14 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *08/30/2001*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

***Claim Objections***

Claims 4, 5, 16, and 17 are objected to because of the following informalities:

In claim 4, line 5, the word "and" must be changed to "or".

In claims 5, 16, and 17, line 4, the word "and" must be changed to "or".

Appropriate correction is required.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1, 3, 4, 7-9, 12, 13, 15, 16, and 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nookala in view of Hobson.

Re claim 9, Nookala discloses a computer system, said computer system comprising:

a graphics controller configured to control a display monitor (column 4, lines 56-64, FIG. 2) and including a logic unit which operates in a working state and a low power-consumption state (column 5, lines 9-11, lines 22-27, FIG. 2, column 7, lines 62-65, column 8, lines 1 and 2) and which consumes less power in the low power-consumption state than in the working state (column 8, lines 4-7, lines 23-27);

a register provided in the graphics controller (FIG. 2, 201, column 12, lines 23-26, FIG. 4) and configured to store state control data for transiting the logic unit to either the working state or the low power-consumption state (column 5, lines 9-12, column 7, lines 62-65, column 8, lines 1 and 2);

a CPU that writes into the register the sate control data designating the low power-consumption state (column 2, lines 41-50, column 5, lines 9-12); and

a state controller provided in the graphics controller (column 5, lines 22-27).

Nookala fails to disclose an operating system performing the power management control and the register written in accordance with an instruction from the operating system. Nookala also fails to disclose the state controller configured to invalidate the state control data designating the low power-consumption state stored in the register, thereby to prohibit the logic unit from transiting to the low power-consumption state from working state.

Hobson teaches the Advanced Configuration and Power Interface (ACPI) specification supporting current operating systems and used for power management (column 2, lines 19-23). Hobson also teaches the operating system

writing sleep requests or messages to the control register in order to place the computer in sleep mode (column 3, lines 5-8, column 4, lines 48-50). Hobson further teaches the computer system utilizing a sleep register and a decoy register implementing the PM1 Control Register as defined by the ACPI specification (column 6, lines 1-9). Immediately after a sleep request is issued by the operating system, the computer system remains in working condition and the transition is prohibited until the devices are configured properly (column 14, lines 52-67, column 15, lines 1-3, lines 7-10). In Hobson the computer system allows for software-based power management control while still permitting hardware-based power management for some legacy devices, thus improving the computer system operation (column 5, lines 41-44, column 6, lines 66 and 67, column 7, lines 1-4). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the operating system power management support, operating system requests/messages and the methodology for prohibiting transfer to sleep mode, as suggested by Hobson with the computer system disclosed by Nookala in order to implement a computer system in which an operating system performs power management control, the register written in accordance with an instruction from the operating system, and the state controller configured to invalidate the state control data designating the low power-consumption state stored in the register, thereby to prohibit the logic unit from transferring to the low power-consumption state from the working state.

Re claim 1, Nookala and Hobson disclose all limitations as per claim 9.

Re claim 13, Nookala and Hobson disclose all limitations as per claim 9. In addition, Nookala further discloses a register configured to be accessed through a bus of the computer and to store state control data designating a state that the device is to assume (column 12, lines 28-30, FIG. 4, column 5, lines 9-11, lines 22-27, FIG. 2).

Re claim 19 and 20, Nookala and Hobson disclose all limitations as per claim 9. In addition, Nookala further discloses controlling the operation of the component of the graphics controller, in order to reduce power consumption of the graphics controller stayed in the working state (column 8, lines 7-14).

Re claim 21, Nookala and Hobson disclose all limitations as per claim 9. In addition, Hobson further teaches invalidating the transit, in accordance with a BIOS (column 4, lines 40-50).

Re claims 3 and 15, Hobson further teaches the graphics controller and device, wherein the state controller has a first mode for prohibiting the logic unit from transiting to the low power-consumption mode (column 14, lines 59-63) and a second mode for allowing the logic to transit to the low power-consumption state (column 14, lines 63-67, column 15, lines 1-3), and the state controller invalidates the state control data designating the low power-consumption state, in the first mode (column 14, lines 59-63).

Re claims 4 and 16, Nookala further discloses the graphics controller and device as per claims 3 and 15, further comprising a register configured to be accessed through the bus of the computer (column 12, lines 28-30) and to store mode-designating data that designates either the first mode or the second mode

(column 5, lines 9-11, lines 22-27, FIG. 2, column 7, lines 62-65, column 8, lines 1 and 2).

Re claim 7, Nookala further discloses the graphics controller, wherein the low power-consumption state is a off state in which the operation of the logic unit is stopped (column 8, lines 35-40).

Re claim 8 and 12, Nookala further discloses the graphics controller and computer system, further comprising a control register configured to be accessed through the bus of the computer and to store control data for controlling a power consumption of the logic unit stayed in the working state (column 5, lines 9-11, lines 22-27, FIG. 2, column 7, lines 62-65, column 8, lines 1 and 2, lines 7-14).

Claims 5 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nookala in view of Hobson, and further in view of Loison.

Re claims 5 and 17, Nookala and Hobson disclose the graphics controller and device as per claims 3 and 15.

Nookala and Hobson fail to disclose an input pin configured to receive from an external device a mode-designating data that designates either the first mode or the second mode.

Loison teaches detecting the presence of a connector-plugged into a Wake on Line (WOL) socket using a switch under the control of BIOS (column 4, lines 11-15, FIG. 2) by temporarily pulling one pin of the socket to a voltage level, and determining the level of the pin (column 3, lines 15-18, FIG. 2). Loison further teaches the switch connected in series between the pin and the level, the pin wired to a register of a controller and means for scanning the register (column

3, lines 18-23, FIG.2, 21). Loison also teaches the pin is a wake-up signal pin (column 3, lines 25 and 26, FIG. 3, 13). In Loison, the methodology for detecting the presence of a WOL connector in a computer ensures that the power consumption of the LAN cards in sleep state will remain bellow the available power (column 3, lines 43-49, column 4, lines 53-59, 62-67). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the pin and methodology, as suggested by Loison with the graphics controller and device disclose by Nookala and Hobson in order to implement an input pin configured to receive from an external device a mode-designating data that designates either the first mode or the second mode.

***Allowable Subject Matter***

Claims 2, 6, 10, 11, 14, and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Re claims 2, 10, and 14, the prior art fails to disclose or suggest the graphics controller, computer system, and device, as per claims 1, 9, and 13, wherein "a switch provided between the register and the logic unit and configured to prohibit the state control data designating the low power-consumption state from being transmitted from the register to the logic unit".

Re claims 6, 11, and 18, the prior art fails to disclose or suggest the graphics controller, computer system, and device, as per claims 1, 9, and 13,

wherein "the selector selects the fixed data while the state controller is operating in a first mode to prohibit the logic unit from transiting to the low power consumption state".

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stefan Stoynov whose telephone number is (571) 272-4236. The examiner can normally be reached between 8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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